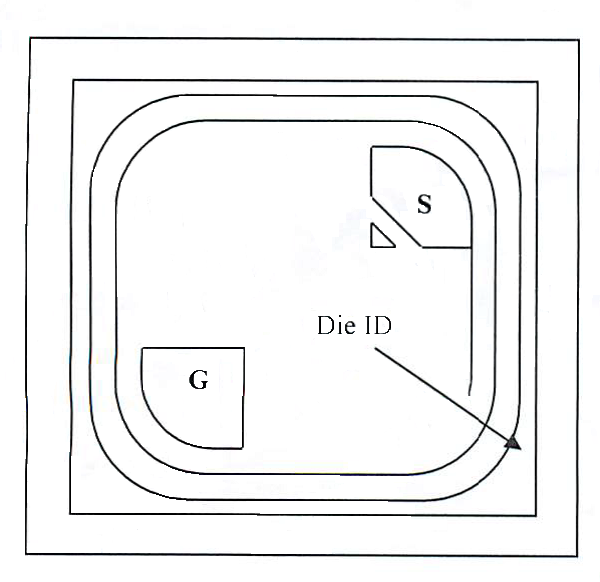
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.025”**



**.025”**

**NOTE: Die backside connection is DRAIN**

**Top Material: Al**

**Backside Material: TiNiAgSn**

**Bond Pad Size: .005” X .005” min.**

**Backside Potential: DRAIN**

**Mask Ref: 9GA**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 4/8/21**

**MFG:FAIRCHILD SEMI THICKNESS .008” P/N: 2N7000**

**DG 10.1.2**

#### Rev B, 7/19/02